REMARKS

The Applicant is filing this Amendment and Response in response to an Official Action dated January 27, 2005. At the time of the Official Action, claims 1-10, 13-16, 18-23 and 26-33 were pending. In this Response and Amendment, claim 32 is amended, claim 34 is added and claim 12 is canceled. Accordingly, claims 1-10, 13-16, 18-23 and 26-34 are currently pending.

The Applicant thanks the Examiner for the acknowledgment that claim 12 would be allowable if rewritten in independent form. As such, claim 12 has been canceled and rewritten in independent form as new claim 34.

In the Office Action, claims 1-4, 7, 9-10, 13, 15-16, 18-23 and 26-33 were rejected under 35 U.S.C. § 103(a) as being obvious based on U.S. Patent No. 6,457,100 to Ignatowski et al. ("the Ignatowski reference") in view of U.S. Patent No. 5,440,7522 to Lentz et al. ("the Lentz reference"). Additionally, claims 5-6 and 14 were rejected under 35 U.S.C. § 103(a) as being obvious based on Ignatowski and Lentz in view of U.S. Patent No. 6,202,127 to Dean ("the Dean reference"). Finally, Examiner rejected claim 8 as being obvious based on Ignatowski and Lentz in view of U.S. Pat No. 5,440,752 to Eng ("the Eng reference"). Each of these rejections is addressed in detail below.

The Rejections Under 35 U.S.C. § 103

In rejecting claim 1 under Section 103 based on Ignatowski in view of Lentz, the Examiner stated:

> Regarding claim 1, Ignatowski discloses a chip-multiprocessing system with scalable architecture (41, figure 3), comprising on a single chip, a plurality of processor cores (15-1 – 15-N, figure 3), a two level cache hierarchy including a first level caches as private cache for each related processor (col. 8 lines 24-35), a second level cache with a relaxed inclusion property (40, figure 3), the second-level cache, i.e., common cache (40, figure 3) being logically shared by the plurality of processor cores (col. 9 lines 8-10), the second level cache being modular with a plurality of interleaved modules (col. 16 lines 33-40 and col. 18 lines 40-46), one or more memory controllers (4, figure 1) capable of operatively communicating with the two-level cache hierarchy and with an off-chip memory (col. 4, line 58 through col. 7 line 24), a cache coherence protocol, one or more coherence protocol engines, i.e., nodal directory, (col. 9 line 64 through col. 10 line 24), an intra-chip switch, i.e., an electronic cross point-type switch, and interconnect subsystem, i.e., inter-node bus. Although Ignatowski differs from the claimed invention in not specifically teaches the first level caches comprising a pair of instruction and data caches. It is well known in the art that the first level cache comprising both data and instruction caches for faster execute and access by the central processor, as an example of Lentz teaches in the multiple processing system (1, figure 1), each processors comprising a data cache 51 and an instruction cache 52 (figure 2 and col. 6 line 65 through col. 7 line 19). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the multiple processing system of Ignatowski in having a pair of data and instruction cache as the first level cache, as per teach of Lentz because it reduces the latency of memory accesses and speed up an access by any processor with their private data and instruction caches.
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> Office Action, p. 3.

The Applicant respectfully traverses the rejection. The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (PTO Bd. App. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221

U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes *all* of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988).

In the present case, the Ignatowski reference fails to disclose all of the claimed elements of the present application. Specifically, independent claim 1 recites a chip-multiprocessing system including "a second level cache with a *relaxed inclusion property*." Independent claim 30 recites a method for scalable chip–multiprocessing, including "a second level cache with a *relaxed inclusion property*." Independent claim 32, as amended, recites a single-chip multiprocessing system, comprising "a second level cache with a *relaxed inclusion property*."

The benefit of employing a relaxed inclusion property is explained in the specification, as follows:

> As a further design strategy, the shared second-level cache has a relaxed or non-inclusion property. Moreover, the PIRANHA™ system incorporates a highly-optimized cache coherence protocol and a novel input/output (I/O) architecture. The design of the shared second-level cache uses a sophisticated protocol that does not enforce inclusion in first-level instruction and data caches in order to maximize the utilization of on-chip caches. Additionally, the CMP system includes an I/O node, a unique I/O architecture, that is a full-fledged member of the interconnect and global shared-memory coherence protocol.
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> Specification, p. 4, lines 3-9.

The application gives additional details about the relaxed inclusion property:

> Since the aggregate capacity of the first-level caches (L1) in the PIRANHA™ system is 1 MB, maintaining data inclusion in the 1 MB second-level cache (L2) can take over and potentially waste the entire L2 capacity with duplicate data. Therefore, the PIRANHA™ system is preferably configures with a relaxed inclusion property or an exclusive cache hierarchy, i.e., non-inclusive cache hierarchy. Although exclusive on-chip cache hierarchies have been previously studied in the context of a single-CPU chip, the use of this technique in the context of a CMP system is yet unexplored. Exclusive on-cache hierarchy in a CMP system leads to interesting issues related to coherence and allocation/replacement policies. To simplify intra-chip coherence and avoid the need for L1 caches lookup, a CMP system such as the PIRANHA™ system keeps a duplicate copy of the L1 tags and state at the L2 controllers. Each controller maintains tag-state information for L1 cache lines that map to it given the address interleaving. The total overhead for the duplicate L1 tag-state across all controllers is less than 1/32 of the total on-chip memory.
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> Specification, p. 13, l. 20 – p. 14, l. 3.

In contrast to the Applicant's claims, the Ignatowski reference discloses a nodal cache system that is only inclusive. The cache system disclosed in Ignatowski does not operate using a *relaxed* inclusion property. As described in the Ignatowski reference:

> Any variety of cache coherent protocols may be used in this single or multiple node computer structure. In the preferred embodiment, *the nodal directory 24 is "inclusive"*, which means that all entries in any L1 directory 3 (which are directly available to the CP on the same processor chip 7) are also contained in the nodal directory 24 which is connected to the respective L1 directories on chips 7.
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> Ignatowski, col. 16, lines 41-47 (emphasis added).
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> Each node 41 in Fig. 4 contains *an nodal directory 24 which is inclusive* of all lines cached in the L1 caches 2 of the CPs 1 in the same node.
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> Ignatowski, col. 19, lines 28-30 (emphasis added).
>
> Because *all nodal directories 24 are inclusive*, any data in an exclusive or modified state in an L1 directory 3 will have that information reflected in its nodal directory 24.
>
> Ignatowski col 20, lines 14-17 (emphasis added).

Thus, the Ignatowski reference does not disclose a system with relaxed inclusion. Rather, the Ignatowski reference discloses a system that has only inclusive properties. Furthermore, nowhere in the Ignatowski reference is the word "relaxed" used.

The Lentz reference is insufficient to overcome this deficiency. The Lentz reference shows a memory control unit (MCU) in the processors of a multi-processor system. The MCU is essentially a switch network for communication between master and slave devices. The switch network arbitrates and prioritizes data requests.

For at least these reasons, the Applicant respectfully submits that independent claim 1, 30 and 32 (and the claims dependent thereon) are not anticipated by Ignatowski. Accordingly, the applicant respectfully requests the withdrawal of the rejection of claims 1-4, 7, 9-10, 13, 15-16, 18-23 and 26-33 under section 103 based on Ignatowski in light of Lentz.

Additionally, claims 5, 6 and 14 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Ignatowski and Lentz as applied to claim 1 and in view of U.S. Pat. No. 6,202,127 to Dean et al ("the Dean reference"). Specifically, the Examiner stated:

> Regarding claims 5-6, the combination of Ignatowski and Lentz differs from the claimed invention in not specifically teaches the chip-multiprocessing system wherein the plurality of processor cores are each capable of executing an instruction set of the ALPHA™ processing core and each configured with a branch target buffer, pre-compute logic for ranch conditions, and a fully bypassed data path. However, Dean teaches such (col. 2 lines 61-65 and col. 3 line 56 through col. 3 line 7). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Ignatowski and Lentz in having the plurality of processor cores are each capable of executing an instructions set of the ALPHA™ processing core and each configured with a branch target buffer, pre-compute logic for ranch conditions, and a fully bypassed data path, as per teaching of Dean, because it implements the chip-multiprocessing system and reduces memory latency.
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> Regarding claim 14, the combination of Ignatowski and Lentz differs from the claimed invention in not specifically teaches the chip-multiprocessing system wherein each of the instruction and data caches is a two-way set-associative cache with virtual indices and physical tags. However, Dean teaches such (col. 3 line 20 through col. 4. line 21). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Ignatowski and Lentz in having each of the instructions and data caches is a two-way set-associative cache with virtual indices and physical tags, as per

> teaching of Dean because it implements the chip-multiprocessing system and reduces memory latency.
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> Office Action, pp. 10-11.

Finally, the Examiner rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Ignatowski and Lentz as applied to claim 1 in view of U.S. Pat. No. 5,467,679 to Eng et al ("the Eng reference"). Specifically, the Examiner stated:

> Regarding claim 8, the combination of Ignatowski and Lentz differs from the claimed invention in not specifically teaches the chip-multiprocessing system wherein the interconnect subsystem includes a network router, a packet switch and input and output queues. However, Eng teaches such (col. 4 line 41 through col. 5 line 31). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the combination of Ignatowski and Lentz in having the interconnect subsystem includes a network router, a packet switch and input and output queues, as per teaching of Eng, because it reduces buffer space and increase throughput is achieved by producing shared memory.
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> Office Action, p. 11.

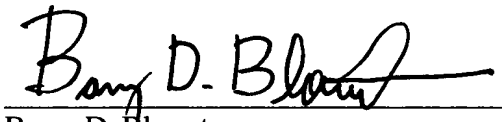
As claim 4-5, 8 and 14 all depend upon independent claim 1, the rejection of these claims under section 103 is defective for at least the reasons set forth above with respect to the rejection of claim 1. Moreover, none of the cited references, Ignatowski, Lentz, Dean or Eng, discloses a chip-multiprocessing system with scalable architecture comprising "a second level cache with a *relaxed inclusion property*." In fact, none of them even contain the word "relaxed." Accordingly, the combination of the cited references cannot render the Applicant's claim obvious. Accordingly, the Applicant respectfully asserts that the rejections of claim 4-5, 8, and 14 under section 103 are erroneous and should be withdrawn.

Conclusion

In view of the remarks set forth above, the Applicant respectfully requests reconsideration of the Examiner's rejections and allowance of all pending claims 1-10, 13-16, 18-23, and 26-34. If the Examiner believes that a telephonic interview will help speed this application toward issuance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,

Date: April 19, 2005



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